Proposal for
the design of a "Low-Power SRAM Using Leakage reduction and Power Management Techniques for Low-power and Energy Applications"
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Description

Over the past decade, applications have seen a growing need for larger memories and storage capacities while simultaneously being less and less power demanding. In SRAMs which are now more prevalent in most systems, while there are multiple factors that affect their overall power consumption, carefully designing each cell can be critical in terms of power consumption reduction. Similarly, while leakage currents may seem relatively small at first sight, they are among the main contributors for SRAMs power consumption. Various leakage reduction techniques have been proposed in the past few years to mitigate and deal with the leakage currents on a circuit level. Different power monitoring techniques have also been proposed to further optimize power efficiency in SRAMs. Our objective in this project is to first investigate a few of the more promising of these methods, combine the novelty and advantage of them into a new and more efficient technique and finally implement that technique in the process provided in the course EE241B.

References

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