Comprehensive and Inclusive Figure of Merit for Comparative Analysis of Different Low-Power SRAM Designs With Leakage Control and Noise Immunity Techniques

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***Abstract*—With the expansion of portable devices, sustainability has become the key factor constraining all systems to consume less and less power, while at the same time maintaining a reasonably satisfying performance and noise immunity during operation. While some metrics are already being used to quantify static random access memory (SRAM) performances, they do not rightfully represent the true performance of the array, and can often be misleading and inaccurate. The new proposed figure of merit (FOM) referred to as noise immunity to power per unit area ratio (NPAR) encompasses the various essential aspects of an SRAM cell and can be used for a more accurate analysis and comparison of different designs. The main notion behind this FOM is that improving either write or read performance while neglecting the other does not translate to an overall improved performance, something that other metrics often fail to demonstrate. Using this proposed FOM, several recent works are briefly evaluated in this paper and fairly compared with respect to each other.**

I. Introduction

To be able to define a practical and reliable figure of merit (FOM) for an SRAM array operation, it is substantial to have a tangible grasp of its main characteristics. Briefly discussed below.

A. Power dissipation

SRAM constitutes a significant portion of the system-on-chip (SoC) area and the growing need for more complex handheld and portable devices drives the need for larger and larger arrays of SRAM in these systems. More so than often, SRAM can be accounted for the most dominant source of a system's power dissipation, and with the size of on-die SRAM arrays increasing at a noticeable rate, the battery-life requirements are becoming more and more challenging to meet. Power dissipation in SRAM resulting from discharging bitlines and various capacitors spread across all corners of the array, as well as the energy dissipated in the logic section of the array and the numerous gates in it, are among the main contributors making up the SRAM array's power consumption. While the aforementioned factors greatly affect SRAM cells' power dissipation, they do not usually worsen dramatically with each node scaling, and their relative effect on the power consumption can be assumed to remain similar, even when scaling occurs. A large number of techniques have been proposed and developed during the past decade to mitigate these issues and provide some alternative methods to overcome the SRAM switching power dissipation problem.

The leakage currents in SRAM are further limiting the power requirements of systems, more pronounced in smaller feature sized technologies. These leakage currents mainly contribute to the standby power dissipation of SRAM cells, further constraining their power consumption performance. To deal with the leakage currents, several techniques have been proposed and implemented in cell design ([1], [2]) reducing their effect on the system's performance.

In terms of SRAM cell's performances, depending on the structure of the cell, the power dissipation for a read operation can vary to some noticeable extent with respect to a write operation. In addition to this, the same operation can result in a different power (or equivalently, energy) consumption when dealing with a 0 value compared to the case of a value of 1. These seemingly intricate and minor details can make the difference between a robust design and a somewhat questionable one and need to be included and accounted for when defining an inclusive metric for SRAM.

B. Noise immunity

Aside from SRAM's power dissipation limiting a system's overall performance, their noise immunity has also great impact on the precision and reliability of the SoC. With the supply voltage gradually scaling down, slowly approaching the threshold voltages of the devices, the margins in which the cells can operate without being disturbed or failing to store or deliver a bit correctly, are becoming tighter than ever before. While some metrics may argue to prioritize read static noise

margin (RSNM) over write margin (WM) or hold static noise margin (HSNM), a fair and reliable way of approaching this would be to take them both into account and include them in the FOM.

C. Access time

Another important aspect of an SRAM array's performance is the access time which directly impacts the speed of the overall system. Similar to the case of the read and write power being distinct of each other, the same situation is also the case when it comes to read-access time and write-access time. The mechanisms which occur at a write operation can significantly differ from the case of a read operation, and consequently, different delays and speed limitations can be engendered and originate from these two operations, and should appropriately be be taken into consideration in the FOM.

D. Area

Beside the dynamic and static features of an SRAM cell array, the other key factor impacting the integration of an SRAM into a system is the area of the array. Due to both dynamic and static performance limitations, the sizing of the transistors in each cell cannot be chosen to be minimized as will, and a number of the devices in the cell are usually not unity-sized, making the cell area larger than anticipated. Moreover, the peripheral circuitry, which includes among other things the read and write driver circuitry, row and column decoders and pre-decoders and, in most cases, read and write assist circuitry as well, can increase the effective area per unit cell, further increasing the total area of the array. Effective area is what masterfully demonstrates the proper area usage of a cell and is essential for it to have a role in the overall performance analysis of the SRAM.

II. State-of-the-art SRAM Cells

A. Schmitt-Trigger-Based (ST-based) SRAM Cell

The Schmitt-trigger-based (ST-based) SRAM cell proposed in [3] makes use of the schmitt-trigger's transfer characteristic to achieve better noise immunity, improving the SRAM's performance. The 4T schmitt-trigger inverter used in the core of the cell is presented in Fig. 1(a) [4]. Technical features of this work include an 11-transistor cell layout, drawn in a 45-nm technology and a nominal supply of 0.5 V. The schematic of the cell proposed in this work is shown in Fig. 2(a). Despite having a single ended write and read operation, which can fairly degrade the write 1 SNM, this work takes advantage of a floating VGND node to address this issue and reduce access time by holding the VGND node of the selected cell floating during the write operation. The timing of the control signals in different modes of operation for this cell are shown in Fig. 2(b).With only the single bitline switching during each operation, the power consumption of the cell is approximately halved, improving the power efficiency of the cell. In terms of cell area, this cell is almost twice as large as a conventional 6T-cell (1.63×1.24), resulting in a more constrained area limit for the array.

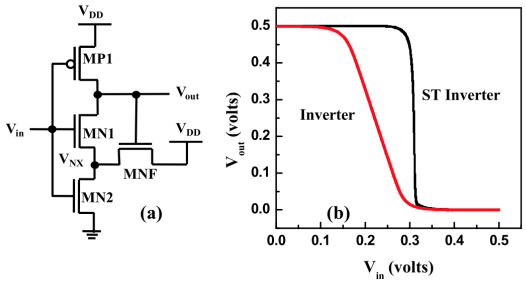

Fig. 1. (a) Basic ST inverter used in [3]. (b) Characteristics of inverter and ST inverter for 0 → 1 transition at the input (V_{dd}= 0.5 V).

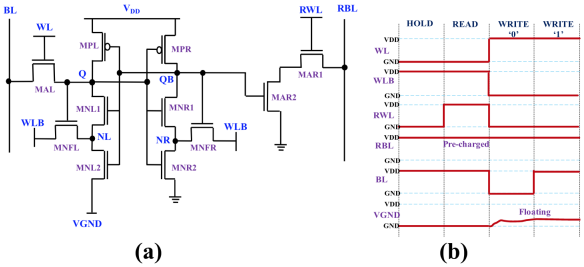

Fig. 2. (a) Schematic and (b) timing of the control signals for the ST11T SRAM cell proposed in [3].

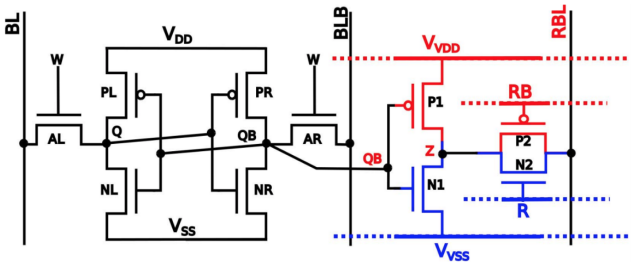

Fig. 3. 10T SRAM cell with row-wise read port dynamic power lines.

B. 10T Cell With Half-V_{dd} Precharge and Row-Wise Dynamically Powered Read Port

Based on 6T SRAM cell, [5] adds a 4T read port for an single ended read shown in Fig. 3. This cell is designed to achieve ultralow leakage. It dynamically controls power rails for read port with V_{VDD} and V_{VSS} as shown in Fig. 4. It precharges RBL to $V_{dd}/2$, charging or discharging from $V_{dd}/2$ for every read operation. Furthermore, the control signals R and RB are boosted to $1.2\times$ nominal signal level to compensate performance degradation due to half-V_{dd} swing. This structure can reduce read power dissipation by 50% compared to a conventional 6T structure.

C. Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture

By using tensile-strained Ge/InGaAs tunnel FET devices, [6] proposes a SRAM structure that can operate under low-voltage ranges ($0.2V \leq V_{DD} \leq 0.6V$). This structure can

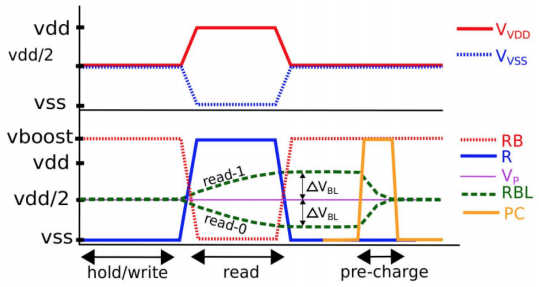

Fig. 4. Levels of control signals during read and otherwise.

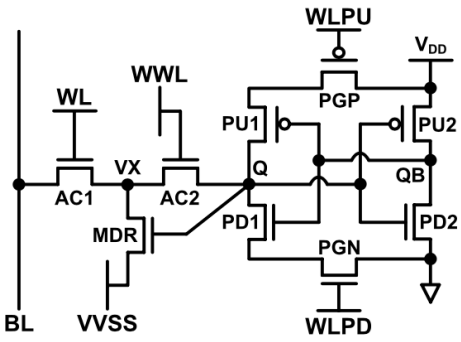

Fig. 5. Power-gated 9T SRAM proposed in [6].

achieve 98% reduction in the cell standby energy consumption by changing Ge strain from 1.5% to 3%. With Ge/InGaAs tunnel FET devices, a simple 7T cell architecture delivers high performance and low-power dissipation at the same time.

D. Power-Gated 9T SRAM Cell for Low-Energy Opertion

The proposed 9T SRAM (Fig. 5) cell in [7] uses bit interleaving to achieve soft error immunity and utilizes a column-based virtual V_{SS} signal to eliminate unnecessary bitline discharges in the unselected columns, leading to reduction of power dissipation.

III. Proposed Metric For SRAM Performance

Considering the fact that recent technologies do not necessarily allow for simultaneously read and write optimization of the cell, more so than often improvements made in one of these two operation cycles will result in a degradation of the other one's performance. For this particular reason, the majority of the SRAM cell arrays are nowadays optimally designed and biased for read operation, and are therefore intrinsically not write-stable. To resolve this issue and accommodate for recent technologies' process limitations and features, write-assist circuits and peripherals are commonly used and implemented as auxiliary circuits to the cell array and accordingly used in the needed mode of operation of the memory cell. This fairly inconvenient interdependency between the read and write stability and optimization which is becoming more pronounced in recent technologies with lower power supply limits, results in a dilemmatic way of approaching the matter of measuring the performance of the cell and array, especially when it comes to power dissipation and access times in different modes of operation.

To put all those interdependencies into perspective and account for a true and comprehensive averaging of both modes' of operation's performances and efficiencies, they need to be accordingly combined and represented in the overall figure of merit.

A. Energy, power and access time

The read and write energies (respectively E_{read} and E_{write}) can be different with respect to each other depending on the structure of the cell and global architecture of the SRAM array. A very low energy consumption for one mode of operation and a relatively larger one for the other does not translate to a high energy efficiency in SRAM since both modes are, to some extent, fairly of similar and equal importance. In dealing with SRAM arrays, it is generally not the most energy-efficient or fastest cycle of operation (read or write) that affects the overall performance of the memory, but rather the one that is more limiting in terms of energy consumption and timing. Therefore, a true averaging method for power would have to be such that the final result be closer to the larger value of the two, rather than just the mean of them. Root mean square averaging exhibits this feature and is therefore used in this metric. To take into account the read and write access times (respectively t_{RA} and t_{WA}) as well, instead of averaging the mere energies of each cycle of operation, their effective power dissipations (energy to access time ratio) is averaged instead.

$$P_{rms} = \sqrt{\frac{\left(\frac{E_{read}}{t_{RA}}\right)^2 + \left(\frac{E_{write}}{t_{WA}}\right)^2}{2}} \tag{1}$$

B. Noise margins

Similar to the case of the energy consumption and access times, the RSNM, WM and HSNM are also all of equal importance and impact in evaluating an SRAM array's performance. However, the most dominant of them would be the one with the smallest value since failure of the cell is more likely to occur in that mode of operation rather the more noise-immune ones. Consequently, when averaging the three margins, the final value should tend to move towards the smaller of them rather their arithmetic mean. The harmonic mean of three values does have this property and is therefore a suitable choice for this case.

$$SNM_{har} = \frac{3}{\frac{1}{RSNM} + \frac{1}{WM} + \frac{1}{HSNM}} \tag{2}$$

C. Area factor

Naturally so, the area of each single cell is a defining and key factor of an SRAM array. However, to account for the peripheral and other auxiliary circuits assisting the cells, and with a conventional 6T-cell as a reference cell for unity area, the area factor is defined as below, and demonstrates the effective area occupied by the each cell in the array.

$$F_{area} = \frac{\textit{Effective area of one cell}}{\textit{Area of a 6T-cell}} \tag{3}$$

TABLE I
STATE-OF-THE-ART SRAM CELL BASIC FIGURES OF MERIT AND NPAR.

Cell Feature	[3]	[6]
Read Energy (aJ)	1250	390000
Read Access Time (ps)	1200	254000
Write Energy (aJ)	53	800000
Write Access Time (ps)	983	$\sim$ 254000
P_{rms} (μW)	0.737	2.5
RSNM (mV)	175	160
WM (mV)	83.5	125
HSNM (mV)	175	160
SNM_{har} (mV)	128.2	146.3
F_{area}	2.02	$\sim$1.24
NPAR (dB)	40.4	38.4

D. FOM

Although an adapted metric and method of comparison might be more preferable in some specific cases, however, the proposed metric can very well demonstrate and depict a comprehensive and all-inclusive measurement of the SRAM cell's performance. This novel metric, called noise immunity to power per unit area (NPAR) captures the essential substance of the SRAM cell's physical and area-related features, power dissipation and access times.

$$NPAR = 10log_{10}(\frac{SNM_{har}^2}{F_{area}P_{rms}}) \tag{4}$$

IV. RESULTS AND DISCUSSION

A. Results and Comparison

2 of the mentioned state-of-the-art SRAM cells are chosen to be compared with the proposed metric. The results are shown in Table I. For the cell presented in [3], due to its single ended structure, the write margin and access time are subsequently different for a value of 1 and 0. Given that the probability of each of them being the value being written into the cell can be assumed equal, their mean value is used to calculate the NPAR.For [6], write access time is not reported, and is here assumed to be equal to the read access time. The area factor reported is the ratio of the proposed cell to 8T cell, so the actual area factor of [6] is a little larger than shown in the table.

As we can see from Table I, NPAR of [3] and [6] is close, but compared with [3], [6] gets higher noise margin and less area at the cost of higher power and lower speed.

B. Discussion

The proposed metric is comprehensive, taking into account almost all key performance parameters of SRAM. This metric can provide an overview of how good a SRAM structure is. By optimizing proposed FOM during designing, an overall performance improvement can be achieved.

However, there are still some limitations for the proposed metric. One of them is that the proposed metric doesn't take PVT-variation tolerance into consideration. In SRAM design, performance at different process corners, temperatures and supply voltage is paramount. The proposed FOM doesn't include terms that indicate variation tolerances, and should therefore be calculated at every corner, temperature, and supply voltage, leading to a large three-dimensional FOM table, which is computationally expensive.

V. CONCLUSION

A novel comprehensive FOM for SRAM has been proposed. Two state-of-the-art SRAM cells are compared with this FOM. The proposed metric does not take into account PVT-variation tolerances and need to be considered across all variation corners. However, it does provides an insightful sense of the SRAM performance in terms of noise immunity, power consumption and area.

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